Non-volatile Memories and Their Space Applications

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Reliability and Radiation Effects on Advanced CMOS Technologies Group
Outline

➢ Introduction

➢ Overview
  ▪ Storage mechanisms
  ▪ Array organization and peripheral circuitry
  ▪ Commercial and space market

➢ Details and radiation effects
  ▪ Charge-based Cells
    • Floating Gate devices
    • Radiation effects on FG cells
    • Radiation effects on peripheral circuits
  ▪ Phase change memories

➢ Conclusions
Non-volatile Memories

- A memory which retains information when powered off

- Key metrics
  - Speed, density, power (cost)
  - Retention: amount of time a memory is able to retain information (e.g., 10 years)
  - Endurance: maximum number of program/erase (read) cycles which can be performed on a memory (e.g., $10^5$ cycles)

- Erase
  - An erase operation may be needed before program
What physical quantity can be used to store information in a non-volatile way?

- **Charge**
  - use a potential well to store charge
  - floating gate, nanocrystals, charge trap (SONOS, TANOS, NROM)

- **Phase**
  - use materials which may be switched from amorphous to crystalline and vice versa
  - phase-change memories (PCM), calchogenide RAM (C-RAM)

- **Dielectric Polarization**
  - use materials that retain their polarization (ferroelectric)
  - Ferroelectric RAM (FeRAM)

- **Magnetization**
  - use materials that retain their magnetization (ferromagnetic)
  - Magnetic RAM (MRAM)

- **Other concepts:**
  - Nanotube RAM (NRAM), Resistive RAM (RRAM), Conductive-bridging RAM (CBRAM), Millipede
Depending on the type of cell, different architectures are possible/needed:

- **Selection device** for each cell
  - PCM, FeRAM, MRAM, …

- **Flash** arrays for charge-based cells
  - NOR: cells in parallel
  - NAND: strings of memory cells (in series), two selection devices for each string of 16/32 cells

- **Crosspoint** (no selection devices)
  - Memory elements at the intersection between bitlines and wordlines, no selection devices!
  - Ideal, best density, but parasitics…
Peripheral Circuitry

- **Row and Column Decoders**: block/page/cell selection
- **Microcontroller/State machine**: executes complex program and erase algorithms
- **Charge pumps**: provide high voltages/currents needed in some memories (e.g., floating gates)
- **Buffers**: always, but may have different sizes
Radiation Effects

- Mix of elements determines radiation sensitivity
  - Storage mechanism
  - Architecture
  - Peripheral circuits elements

- Rules of thumb
  - Cells may be hard, but periphery may be soft
  - **Charge** based cells more sensitive
  - When **high voltages** are needed for program/erase (or even read) operations, radiation sensitivity gets worse
NAND FLASH Scaling Trends

Storage capacity (Mb)

Cond. 1Mb
ISSCC, VLSI Circuits, ASSCC
IEDM, VLSI Tech.

NAND flash
128Gb
32Gb
RRAM

PRAM
FeRAM
128Mb
8Gb

MRAM
64Mb

100,000
10,000
1000
100
10
1

2001 2003 2005 2007 2009 2011 2013
Year
Mainstream Market

- **Large (ever-increasing) capacity**
  - now **128 Gbit at 16 nm**, larger than SDRAM, and pushing Moore’s law, ahead of microprocessors; **3-D chips** (V-NAND)

- Non-volatile’s are a growing share of the semiconductor memory market (Digital cameras, MP3 Players, …)

- So far dominated by **Flash Floating Gate (FG)** technology

- **How long will survive FG/Charge-based beyond 20nm?**

- **Radiation Sensitivity**
  - **Low** (100 krad or less, SEFI, SEU, SEL) because of cells (FG) and peripheral circuitry (all)

- **Possible replacements** (short/medium term?)
  - Phase change memories (good for radiation) for the NOR architecture
Rad-hard Memories

- **Small** capacity
  - Few Mbits, typically <64 Mbit

- **Technologies**
  - Charge Trap/SONOS devices
  - Magnetic RAM (MRAM)
  - Phase Change/Chalcogenide RAM (C-RAM)
  - Ferroelectric (FeRAM)

- **Radiation Hardness**
  - ~ Mrad
  - Robust cells (intrinsically or because of large feature size)
  - Rad-hard peripheral circuitry

- **Future**
  - *Nanotube-based memories? …*
For space storage applications, flash NVMs feature:

- the highest available storage density → substantial savings in mass and volume occupancy
- when in idle state, they may be kept unbiased without losing data → energy saving
- In case of device functional interrupts, power cycling can be used to restore the correct functionality without any data loss

Yet, NVMs suffer, in comparison with SDRAM, of:

- moderate data transfer rate
- program/erase only at page/block level
- limited endurance (10^5 cycles)
Flash NVMs are not ideal for the **workspace memories**:
- They cannot grant fast random access to small data entries

Instead, NVMs are the right choice for **mass storage applications**:
- Mass memories typically buffer data entities of many kbytes without any need for data modification
- The frequency of write accesses to the same storage location is often rather low, less than 10 write accesses/day \( \rightarrow \) less than \( 3.6 \cdot 10^4 \) operations within 10 years (i.e., less than 60% of the endurance window)
- Wear-out issues can be mitigated by more storage capacity. Further, wear leveling distributes the storage locations rather uniformly over the address space, with integrated bad block management
Storage concept: Inject or remove charge between the control gate and the channel, for instance in a floating gate.

Charge storage element: floating polysilicon gate (FG), charge-trap layer, nanocrystals.
Charge-based Cells

Floating Gate

Control Gate

DrainSource

Interpoly
dielectric

Tunnel
oxide

Source

Control Gate

Drain

Floating Gate

CHARGE STORAGE ELEMENT
The presence of electrons/holes in the charge-storage element alters the device threshold voltage.

**Read:** sense the drain current at a proper gate bias and compare it with a reference current.

\[ Q^+ \Rightarrow V_{th} \downarrow \quad Q^- \Rightarrow V_{th} \uparrow \]
History

- **1967**: first proposal of Floating Gate memory (Kahng & Sze)
- **1971**: Electrical Programmable Read Only Memory (**EPROM**) is invented, after investigations of faulty MOSFET where the gate connection had broken (Frohman)
- **1978**: Electrically Erasable ROM (**E²PROM**) is introduced (Perlegos)
- **1985**: First attempts to build a **NOR Flash** memory
- **Mid 1990s**: **NAND Flash** enjoys commercial success
- **2003**: NAND Flash overcomes NOR in terms of volumes

State-of-the-art

- NAND: 16-nm 128 Gbit
- NOR: 45-nm 8 Gbit multi-level

Future

- Replacements are needed because development of FG cells is rapidly approaching scaling limits, but some countermeasures are already in place: **3-D NAND memories**!
Floating Gate (FG) potential is the key
- Coupling with the other terminals

FG device equations can be obtained by substituting gate voltage with floating gate voltage in standard MOSFET’s equations

Important differences
- Drain turn-on
- No saturation with $V_D$ occurs

$\Delta V_{th} = - \frac{Q_{FG}}{C_{PP}}$

$V_{FG} = \alpha_G(V_G - \Delta V_{th}) + \alpha_D V_D + \ldots$

$\alpha_G = \frac{C_{PP}}{C_{PP} + C_D + \ldots}$

$\alpha_x$ are coupling coefficients
FG: Band Diagram

Cell structure
Control gate
Floating gate
Source
Tunnel Oxide ~10 nm
Drain

Blocking ONO

Ideal energy band diagram

Erased
Programmed
Injection/Removal Mechanisms

- **Channel hot electrons (holes)**
  - Carriers are heated in the channel and acquire enough energy to surmount the potential barrier
  - Efficiency is low, a lot of drain current for a just a few injected carriers

- **Fowler-Nordheim tunneling**
  - Quantum-mechanical tunneling. The carriers do not have the energy classically needed to overtake the potential barrier
  - Slower than CHE/CHH

- **(UV exposure)**

- **High voltages** are required
  - charge pumps are needed to generate high voltages for single supply operation
Threshold Voltage Distributions

- Especially with large arrays, the **statistical distributions** of parameters are extremely important.

![Diagram](image)

- **Read voltage**
- **Ideal distributions**

\[ V_{th} \text{ [V]} \]

**Cell Distribution**

- Log[#]
Threshold Voltage Distributions

- Especially with large arrays, the statistical distributions of parameters are extremely important.
- $V_{th}$ distributions are typically gaussian.
- Tightening program/erase algorithms are used.
- Behavior of tail bits may be dominant.
- Distributions are not visible to the end-user, only digital values.

**Actual distributions**

Cell Distribution

<table>
<thead>
<tr>
<th>Log#</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read voltage</td>
</tr>
<tr>
<td>“1”</td>
</tr>
<tr>
<td>“0”</td>
</tr>
<tr>
<td>Erase verify</td>
</tr>
<tr>
<td>Program verify</td>
</tr>
<tr>
<td>$V_{th}$ [V]</td>
</tr>
</tbody>
</table>

S. Gerardin, SERESSA 2015
More than one bit per cell can be stored, by modulating the amount of charge injected in the floating gate.

Rely on tight statistical control of $V_{th}$ distribution.

More complex (and slower) program algorithms.

Increased density, lower cost but poorer performance and reliability.

Cell Distribution

<table>
<thead>
<tr>
<th>Log#</th>
<th>L0</th>
<th>L1</th>
<th>L2</th>
<th>L3</th>
</tr>
</thead>
<tbody>
<tr>
<td>&quot;11&quot;</td>
<td>&quot;10&quot;</td>
<td>&quot;00&quot;</td>
<td>&quot;01&quot;</td>
<td></td>
</tr>
</tbody>
</table>

$V_{th}$
Array Architecture

- **Electrically Programmable ROM (EPROM)**
  - Erasable through UV exposure

- **Electrically Erasable and Programmable ROM (E²PROM)**
  - Erasable at the single cell level
  - Requires a selection device for each cell ⇒ density penalty

- **Flash arrays**
  - Erasable in blocks
  - No/few selection devices
  - Higher density
  - Combine the best of EPROM (density) and EEPROM (usability)
NOR

- Cells in parallel, bit size ~ 10 $F^2$ ($F =$ Feature size)

- Performance
  - Fast random access ~100 ns
  - Word program ~ 5 $\mu$s
  - Block (Mb) erase ~200 ms

- Applications
  - Read-mostly memory
  - Code storage
NOR Operation

Program

- Channel hot electrons
- WL high & BL high & SL GND
- High programming HC current ⇒ low parallelism
NOR Operation

- **Program**
  - Channel hot electrons
  - WL high & BL high & SL GND
  - High programming current $\Rightarrow$ low parallelism

- **Erase**
  - FN tunneling
  - Low WL & high SL & float BL
  - Sequence of pulses, erase verify $\Rightarrow$ reliability margin
NOR Operation

- **Program**
  - Channel hot electrons
  - WL high & BL high & SL GND
  - High programming current ⇒ low parallelism

- **Erase**
  - FN tunneling
  - Low WL & high SL & float BL
  - Sequence of pulses, erase verify ⇒ reliability margin

- **Read**
  - WL on & sense BL
  - ECC may be present in MLC
NAND

- Cells arranged in strings (16/32), bit size ~ 4F²
- The smallest feature size!
- Source Selection Line (SSL), and Drain Selection Line (DSL) devices for each 16-32 FG string

Performance
- Series arrangement, - speed, + density and parallelism
- High throughput ~ 40MB/s
- Page (kB) program ~0.2 ms
- Block (MB) erase ~2ms
- Compulsory use of ECC

Applications
- Used for data storage
NAND Operation

Program
- FN tunneling
- Selected WL very high & other WL’s high & BL GND
NAND Operation

- Program
  - FN tunneling
  - Selected WL very high & other WL’s high & BL GND

- Erase
  - FN tunneling with reversed polarity
NAND Operation

- **Program**
  - FN tunneling
  - Selected WL very high & other WL’s high & BL GND

- **Erase**
  - FN tunneling with reversed polarity

- **Read**
  - Unselected WL’s biased at $V_{\text{read}} \Rightarrow$ both erased and programmed cells are on at $V_{\text{read}}$
  - Selected WL biased at 0V $\Rightarrow$ only erased cells are on
  - ECC needed
Reliability of FG’s

- **Complex and critical**
  - Intrinsic phenomena occurring in all cells in a uniform way
  - Single-bit failures occurring just in a few bits out of a large number of cells, due to
    - extrinsic defects (particles)
    - unfortunate configurations (alignment) of intrinsic point defects

- **Endurance**
  - Limited by generation of traps and charge trapping during high-voltage operations (10 MV/cm) in the tunnel oxide
  - Typical = $10^5$ cycles

- **Retention**
  - Limited by Stress induced leakage current
  - Typical = 10 years
FG: Radiation Effects

- Until a few years ago...
  - Only effects in the peripheral circuitry were of concern
  - Charge pumps weakest component
- …but nowadays
  - Effects in the peripheral circuitry are still very important
  - but FG array sensitivity is an issue as well
- TID
- SEEes on:
  - Cells
  - Periphery:
    - Page buffer
    - Microcontroller
When the threshold voltage shift is large enough to bring the cell beyond the read voltage, an error occurs.

Intermittent errors may take place when $V_{th}$ close to read voltage.
Uniform shifts of the $V_{th}$ distributions

Movement towards the intrinsic distribution, i.e., the one the cells would have with no net charge in the FG $\Rightarrow$ discharge of the FG

Typical doses for errors $\sim n \times 10$ krad(Si)

Dosimeters?

G. Cellere, et al., TNS 2004
Device irradiated during read cycles: $V_{th}$ distributions and errors build-up as a function of accumulated dose

Errors at the output pins

$V_{th}$ distributions

M. Bagatin, et al., TNS 2009
Device irradiated during read cycles: $V_{th}$ distributions and errors build-up as a function of accumulated dose.
Device irradiated during read cycles: \( V_{th} \) distributions and errors build-up as a function of accumulated dose.

M. Bagatin, et al., TNS 2009

Errors at the output pins

\( V_{th} \) distributions

Programmed ("0")

Erased ("1")
Device irradiated during read cycles: $V_{th}$ distributions and errors build-up as a function of accumulated dose.

$V_{th}$ distributions and errors build-up as a function of accumulated dose.

Errors at the output pins.

M. Bagatin, et al., TNS 2009
Device irradiated during read cycles: $V_{th}$ distributions and errors build-up as a function of accumulated dose.

$V_{th}$ distributions

Errors at the output pins

M. Bagatin, et al., TNS 2009
Device irradiated during read cycles: \( V_{th} \) distributions and errors build-up as a function of accumulated dose

\( V_{th} \) distributions

Errors at the output pins

M. Bagatin, et al., TNS 2009
No errors are observed in erased cells because the neutral distribution is below $V_{\text{ref}}$ in these devices.

Errors at the output pins

$V_{\text{th}}$ distributions

M. Bagatin, et al., TNS 2009
FG: TID Basic Mechanisms

- Three basic mechanisms:
  1. Charge injection in the FG
  2. Charge trapping in the tunnel oxide
  3. Internal Photoemission

- Effects do not depend much on scaling (remember oxides can hardly be scaled because of reliability)
Flash: Charge Pumps Radiation Effects

Degradation of program charge pump in a NAND Flash memory

- **TID**, shift in the threshold voltage
  - Failure dose usually < 100 krad
- **Single Event Gate Rupture**, rupture of the gate oxide
- One of the most sensitive building blocks

![Graph showing degradation of program charge pump](image)

*M. Bagatin, et al., TNS 2009*
Use cases

1. **Mostly off**: memory off most of the time and powered at regular intervals (about 2 krad), during which operating and retention tests are carried out.

2. **Low duty**: memory powered in the selected state (ready to operate) and exercised at regular intervals (about 2 krad), during which operating and retention tests are carried out.

3. **High duty**: memory continuously operated through a sequence of E/R/P/R operations with no dead time. Every 10 E/R/P/R cycles a retention test is carried out.
Total Dose Fails in SLC memories

- **Failure criteria**
  - Retention: 1% of bit corrupted
  - Erase: failure to erase a block
  - Program: failure to program a page

- **In SLC**
  - Retention failures independent of operating conditions
  - Erase and program fails occur later when memory is mostly off

Failure levels for 34-nm SLC NAND Flash manufactured by Micron

*S. Gerardin, et al., TNS 2010*
Total Dose Fails in MLC memories

- **Retention errors**
  - Occur at a higher rate than in SLC and earlier than P/E fails

- **Program/Erase**
  - Failure levels lower than SLC
  - Contrary to SLC, mostly-off and low duty are almost equivalent conditions for this type of failures
  - High duty most severe condition

Failure levels for 25-nm MLC NAND Flash manufactured by Micron

S. Gerardin, et al., TNS 2010
**A secondary peak appears in the distributions right after exposure to heavy ions**

- Distance between the two peaks is average $\Delta V_{th}$
- Height of the peak (number of cells in the secondary distribution) related to the number of struck FGs

---

[G. Cellere, et al., TNS 2001]
A transition region appears in the distributions between the primary and secondary peaks.

Such region is correlated to energetic delta electrons emitted by the ion hitting outside the FG cell area.
Charge loss \textbf{linearly dependent} on
- electric field
- LET

Not dependent on charge yield!

\textbf{Strong function of scaling}: the smaller the FG, the more severe the effect

\begin{itemize}
  \item \(\Delta V_{th}\) is linearly dependent on electric field and LET.
  \item Not dependent on charge yield.
  \item Strong function of scaling: the smaller the FG, the more severe the effect.
\end{itemize}

\textit{G. Cellere, et al., TNS 2004}
FG & Heavy Ions: LET and Electric Field (2)

- Charge loss **linearly dependent** on
  - electric field
  - LET
- Not dependent on charge yield!
- **Strong function of scaling**: the smaller the FG, the more severe the effect

G. Cellere, et al., TNS 2004
Charge loss linearly dependent on:
- electric field
- LET

Not dependent on charge yield!

Strong function of scaling: the smaller the FG, the more severe the effect.

Heavy ion strikes can discharge the FG:
- Transient conductive path
- Transient carrier flux

**Transient** leakage path due to high density of electron/hole pairs created by radiation.
Angular effects of heavy ions

- What happens when changing the irradiation angle? In real world (e.g., space) the ion flux is ~isotropic

- After 1217-MeV Xe irradiation

At 75° more than 20 FGs corrupted by a single ion!

Cellere et al, TNS 2007
Heavy-ion Induced $V_{th}$ Tails

Heavy ions collectively produce:

- **Secondary Peak:** the number of cells is in good agreement with the number of strikes going through FGs
- **Transition Region:** origin not yet completely clear

65-nm Micron NOR Flash memories irradiated with $3 \cdot 10^7$ cm$^{-2}$ Silicon ions ($E=121$ MeV, LET=9.8 MeV·cm$^2$·mg$^{-1}$)
Geant4 Application

- 65-nm NOR devices were modeled in 3D
- Heavy-ions and neutrons strikes were simulated
- Simulations provide energy deposition in the floating gate and in the tunnel oxide of particles crossing cells
The experimental data and the energy deposition can be experimentally related through a $\Delta V_{\text{th}}(\text{LET})$. 

65-nm NOR irradiated with Ni
The experimental $\Delta V_{th}$ vs LET can be fitted with a simple relation, either a power law or linear relation.

- Linear relation with non-zero intercept is non-physical.
Agreement is much better when considering energy deposition in the FG as opposed to the tunnel oxide.

Width of the secondary peak related mostly to variability in energy deposition.
In addition to the large energy depositions caused by ions going through FG (large events)...

there are several small depositions by energetic electrons going through FG (small events), we can think of them in terms of total dose.
The experimental $\Delta V_{th} vs \ TID$ can be fitted with a simple linear relation.

The extracted conversion coefficient is 15.4 mV/krad.

If we weigh the small events with this number…

Experimental data on 65-nm NOR Flash memories irradiated with x rays.
A good agreement is obtained with different ions.
Even though, the oxides surrounding the FG are quite thin (8.5 nm in NAND FG) charge trapping can take place.

Removal of trapped charge may cause some errors to disappear both after TID and heavy-ion exposures.

*Silver* $E=266$ MeV, $LET=57$ MeV cm$^2$/mg

*M. Bagatin, et al., TNS*
FG & Heavy Ions: Permanent Leakage Paths

- In addition to prompt discharge, permanent damage can occur.
- Cells hits by high-LET heavy-ions and then reprogrammed, experience a charge loss over time.
- Caused by permanent defects in the tunnel oxide leading to Radiation-Induced Leakage Current (compare with SILC).

Permanent leakage path due to defects created by radiation.
Radiation Effects on $V_{TH}$ distributions

- Large tails after irradiation
- Number of bits in tail does not depend on ion LET (it depends on fluence)
- $\Delta V_{TH}$ strongly depends on ion LET

- These cells (hit) only are considered in the next experiments
Data retention in hit FG cells

- Hit devices only were re-programmed
- After only 30min a clear tail appears…
- …which increases more and more with time

After 20 days, $\Delta V_{TH} \sim 4V$!!!
Model vs. Experimental

- **Model**: multi-trap assisted tunneling current through tunnel oxide
- **Experimental data** obtained from 0.04μm² device irradiated with I previously shown
- **Bars** → variance (spread) of experimental data
- **Lines** → calculations

- With **20 defects in the tunnel oxide**, good agreement on:
  - Mean value
  - Extreme values (spread)
Typical errors during read operation under exposure to heavy ions

- Static errors, linked to FG cells
- Dynamic errors, linked to the peripheral circuitry
- Single Event Functional Interruptions, due to strikes in the microcontroller memory

*M. Bagatin, et al., TNS 2008*
In the NAND architecture a large page buffer (PB) is present.

A page is transferred from (to) the FG array into the PB before (after) being read (written) at the pins.
In the NAND architecture a large page buffer (PB) is present. A page is transferred from (to) the FG array into the PB before (after) being read (written) at the pins.
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In the NAND architecture a large page buffer (PB) is present.

A page is transferred from (to) the FG array into the PB before (after) being read (written) at the pins.

While in the PB, data are sensitive to radiation ⇒ Dynamic Errors.
### Flash: Single Event Functional Interruption

**Strikes in the microcontroller** may lead to inconsistent states
- Read fails on whole pages/blocks
- Program/Erase failure

Functionality can usually be restored through:
- Repeat operation
- Reset
- Power-cycle

<table>
<thead>
<tr>
<th>Error Type</th>
<th>Description</th>
<th>Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Block-erase SEFI</td>
<td>The device’s ready signal never exits the busy state.</td>
<td>Reset power only.</td>
</tr>
<tr>
<td>Partial erase SEFI</td>
<td>Block-erase suspends at the first address. Few blocks are erased.</td>
<td>Repeat the erase process.</td>
</tr>
<tr>
<td>Write SEFI</td>
<td>Write operation completion’s status suspends</td>
<td>Reset power only.</td>
</tr>
<tr>
<td>Read SEFI</td>
<td>Sensing circuitry suspends due to charge built-up. Next read operation doesn’t clear errors.</td>
<td>Repeat the read process or cycle power.</td>
</tr>
<tr>
<td>Irregular SEFIs</td>
<td>Read operation locks into endless loop. Write operation stops.</td>
<td>Reset power only.</td>
</tr>
</tbody>
</table>

*D.N. Nguyen, et al., REDW2002*
Future Memories

- **Phase change memories**
  - Phase Change Materials (e.g., chalcogenides) can be electrically switched between the *amorphous* and *crystalline* state, through Joule heating.
  - These two states feature one or two orders of magnitude of difference in resistivity, which can be sensed with a proper scheme.

- **Nanotube RAM (NRAM)**
  - Cell: single walled nanotube suspended over an electrode.
  - “0” = suspended “1” = in contact (van der Waals forces).
  - Great potential for radiation hardness.

- **Resistive RAM (RRAM)**
  - Based on materials whose resistivity can be changed electrically, with a breakdown-like path.
  - Good scalability, cross-point arrays.

- **Conductive-bridging RAM (CBRAM, PMC)**
  - Relocation of ions inside an electrolyte.
  - Presence or absence of a nanowire between two electrodes.

- **Millepede**
  - Use pits in a polymer material created with a MEMS-probe.
  - Great scalability.
Phase Change Memories

- **Memory Cells**
  - Based on the reversible phase transition of a chalcogenide material Ge$_2$Sb$_2$Te$_5$ (GST):
    - amorphous $\leftrightarrow$ XTL
    - RESET $\leftrightarrow$ SET

![Diagram showing the reversible phase transition and electrical characteristics of Phase Change Memories.](image)

- Temperature $T_{\text{melt}}$ and $T_{\text{crys}}$
- Current $I$ vs. Voltage $V$
- Time $t$ vs. Phase-Change
- Crystalline and Amorphous states
- Read and Write operations
Phase Change Memories

- **Periphery**
  - Many of the same issues as in standard CMOS circuits, but it may be hardened by design/process

- **Memory Cells**
  - Believed to be hard and totally immune to radiation effects, because storage mechanism is not based on charge
  - As we will see that’s not entirely true
Neutron Results

- Devices in retention mode (i.e. off)
- No significant increase in bit errors caused by neutrons, regardless of pattern

Irradiated with neutrons @ ISIS

S. Gerardin, SERESSA 2015
Heavy Ions along the Bit line

- Highest used LET(Si) = 59.2 MeV·mg⁻¹·cm²
- High fluence = 3·10⁷ ions/cm²
- No significant increase in bit errors

45-nm PCM

Irradiated with 267-MeV iodine @ SIRAD

S. Gerardin, SERESSA 2015
Heavy Ions along the Word line (1)

- Highest used LET(Si) = 59.2 MeV·mg⁻¹·cm²
- High fluence 3·10⁷ ions/cm²
- Large increase at high incidence angles > 40°
- Errors only in cells set to ‘1’ prior to the exposure (crystalline)

45-nm PCM

<table>
<thead>
<tr>
<th>Irradiation angle along WL [°]</th>
<th>Bit error rate [post rad/ pre rad]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>20</td>
</tr>
<tr>
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<td>30</td>
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<td>40</td>
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<tr>
<td></td>
<td>60</td>
</tr>
<tr>
<td></td>
<td>70</td>
</tr>
<tr>
<td></td>
<td>80</td>
</tr>
</tbody>
</table>

Cells set to ‘1’.
Irradiated with 267-MeV iodine @ SIRAD

S. Gerardin, SERESSA 2015
Heavy Ions along the Word line (2)

45-nm PCM

- Threshold LET \( \geq 40 \text{ MeV} \cdot \text{mg}^{-1} \text{ cm}^2 \)
- Consistent with neutron results: no effect expected

Cells set to ‘1’.
Irradiated @ SIRAD

S. Gerardin, SERESSA 2015
Current Distributions

- Errors only in cells set to ‘1’ prior to the exposure (crystalline)
- About one order of magnitude between the lower edge of the ‘1’ current distribution and the upper edge of the ‘0’ distribution

Representative pre-rad current distribution
Cell Design

- Cell is asymmetrical
- In particular, the heater section has one litho-driven dimension and one sub-litho dimension
- The interface between the heater and the chalcogenide material is rectangular, with the long side oriented along the word line
- Damage at the heater/GST interface

Cartoon of a PCM cell (not to scale)
Energetic heavy ions can create latent tracks of damage in several materials, including insulators and semiconductors.

**Thermal spike model:** due to electron-phonon coupling, a heavy ion heats the material in a small cylinder around its trajectory, causing the melting temperature to be locally reached.

No data exist for Ge\(_2\)Sb\(_2\)Te\(_5\), and no general rules are available to predict latent track formation.

Due to the quick cooling, the GST material may be amorphized after the heavy-ion strike!
Conclusions

- Non-volatile memories have been dominating the commercial market
- They have become more and more appealing for space applications, thanks to their non-volatility and high density, not matched by rad-hard components
- Yet, these devices are sensitive to both TID and SEEs, in both the cell arrays and peripheral circuitry
- They are intensively studied, in order to evaluate the more resilient devices and, correspondingly, the best conditions for their use in different radiation environments
- New unexpected effects may appear due to nano-size!
Atmospheric neutrons

- Not charged, they do not directly ionize materials
- They can give rise to secondary charged byproducts (= heavy ions) by interacting with chip materials
- Wide range of energies
- The generated charge particles have a wide distribution of LETs
Atmospheric-like neutrons produce:
- Secondary charged byproducts
- Linear $V_{th}$ tails in log-lin scale

65-nm NOR Flash memories irradiated with $3.6 \times 10^{10}$ cm$^{-2}$ neutrons with atmospheric-like spectrum
Neutrons

- Geant4 used to assess neutron byproducts, heavy-ion and x-ray data for conversion coefficients.
- Small events fit the tail at lower $V_{th}$.
- Large events fit the tail at higher $V_{th}$.
- Good agreement despite limitations (energies, angles of heavy ions used for conversion).

Tail on L3 for 65-nm NOR Flash memories irradiated with $3.6 \times 10^{10}$ cm$^{-2}$ neutrons with atmospheric-like spectrum.
The number of errors due to neutrons is significantly larger than pre-rad errors during our accelerated tests.

- $\sigma$ exponentially increases as the cell feature size is reduced.
- The FG error bit $\sigma$ (averaged on all levels) for 25-nm samples is more than one order of magnitude larger than for 50-nm samples.

Non-zero error rate (pre-rad errors) even without radiation, due to read and program disturb, erratic tunneling, stress induced leakage current, etc.

$$\sigma = \frac{\#\text{pre-rad_errors}}{\text{fluence} \cdot \#\text{bits}}$$
- 34-nm SLC (vendor A) is one of the first generations of single-bit cells to be sensitive to neutrons
- Errors are all ‘0’ to ‘1’ flips (programmed to erased)
- The neutron cross section of 34-nm SLC is more than 3 orders of magnitude smaller with respect to 25-nm MLC samples
Model: Neutron Scaling Trends

- Through the modeling of threshold LET, neutron cross section is modeled and fitted to our experimental data.
- A turnaround is expected between 10 and 20 nm:
  - For one or few more generations we expect the neutron $\sigma$ to increase.
  - Afterwards a significant decrease should occur, due to the fact that the FG becomes smaller and smaller than the heavy-ion track.

*M. Bagatin, et al., TNS 2014*
Alpha FG error cross section

- For MLC samples the alpha error $\sigma$ is about 3 orders of magnitude larger with respect to the neutron error $\sigma$
- From 50-nm MLC devices to 25-nm ones, the error sensitivity increases by almost 2 orders of magnitude
- The most scaled SLC samples we tested (34 nm) are not sensitive to alpha particles yet

- MLC and SLC samples by vendor A irradiated with $^{241}$Am alpha particles
- Empty symbols indicate the observability limit of events after a fluence of $3 \cdot 10^7$ cm$^{-2}$