reflector using dual-slot antennas, Electron Lett 34 (1998), pp. 1374-1376.
4. M.G. Christodoulou and D.P. Chrissoulidis, 2D Van Atta retrodirective array using dual polarized two-port square microstrip patches, International Conference on Antennas and propagation, April 17–20, 2001, IEE, 2001, Conference Publication No. 480.
5. W.-J. Tseng and S.-J. Chung, A planar Van Atta array reflector with retrodirectivity in both E-plane and H-plane, IEEE Trans Antennas Propag 48 (2000).
6. M. Fujita and C. Murakami, Experimental study of a polarization-rotating Van Atta array with reduced co-polarized radar cross-section, Geoscience and Remote Sensing Symposium, 2003 IGARSS'03, Proc 2003 IEEE Int 7 (2003), 4503-4505.

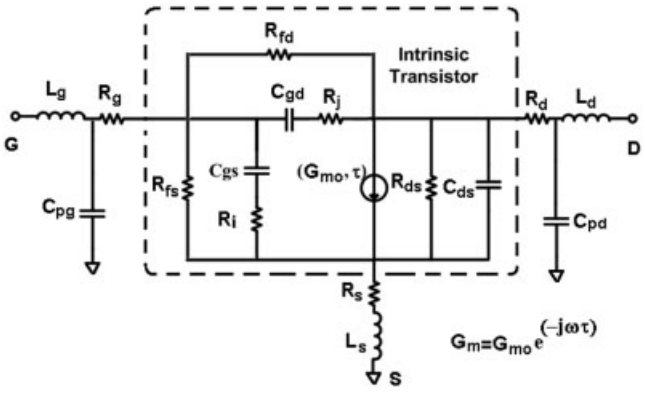

Figure 1 Small-signal equivalent circuit model

A NEW ANALYTICAL METHOD TO EXTRACT THE SMALL-SIGNAL EQUIVALENT CIRCUIT OF HIGH FREQUENCY FET TRANSISTORS

J. L. Olvera Cervantes, J. L. Medina Monroy, R. A. Chávez Pérez, and A. Velázquez Ventura
Electronic and Telecommunication Department, CICESE Research Center, Km 107 Carretera Tijuana-Ensenada, 22860 Ensenada, B. C., México

Received 14 July 2007

ABSTRACT: *A new set of simply analytical equations is proposed as an alternative method to calculate the intrinsic transistor elements of an extended model for microwave FET's. This method is based on Y-parameters as well as on a new process to determine the differential resistances R_{fs} and R_{fd}, including the frequency effect, in such way that measurements at very low frequencies are not required and long iterative methods are avoided. The method was applied to FET's transistors and the validity of the model is certified by direct comparison with measured data from 1 to 45 GHz.* © 2007 Wiley Periodicals, Inc. Microwave Opt Technol Lett 50: 453–457, 2008; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.23130

Key words: *FET's; transistor model; equivalent circuit; intrinsic transistor*

1. INTRODUCTION

A simple and accurate method for extracting the small-signal equivalent-circuit model of high frequency FETs transistors is required, becoming very important for evaluation of transistor microwave performance and the design of monolithic microwave integrated circuits (MMICs).

Generally, the equivalent-circuit model elements are divided in two circuits: the extrinsic or parasitic transistor elements (that not depend on bias) and the intrinsic transistor elements (that are bias dependent). Figure 1 depicts the extended equivalent circuit model for FETs. Here, C_{pg}, C_{pd}, L_g, L_s, L_d, R_g, R_s, and R_d represent the eight external parasitic-pad effects, and the 10 elements: C_{gs}, C_{gd}, C_{ds}, R_j, R_{fd}, R_i, R_{fs}, R_{ds}, G_{mo} and τ correspond to the intrinsic transistor. It is important to mention that in [1, 2] the intrinsic transistor is modeled by seven elements only, while the extended circuit model proposed in [3] and shown in Figure 1, includes three additional elements (R_j, R_{fd}, R_{fs}). In this model, R_j is added to C_{gd} to make the circuit symmetrical in reference with drain and source. Additionally, the differential resistances of the gate diodes (gate-to-source and gate-to-drain diodes), are modeled by the resistances R_{fs} and R_{fd}, respectively, having a tendency to improve the model at low frequencies.

Typically, the extraction process is divided into two stages: the first stage is dedicated to determine the extrinsic elements, while the second stage to obtain the intrinsic elements. Methodologies to determine and remove the parasitic pad effects can be classified as methods that are based on special test structures and those that based on forward and reverse bias measurements. In [1, 4-10], different methods to remove the parasitic-pad effects in FET's and HBT's were proposed. Some methods using open/short test structures were presented in [6] and [10], while others based on forward and reverse bias measurements are given in [1-3, 11].

Once the extrinsic elements are determined, a suitable deembedding process is applied to remove the parasitic pad effects, to determine the intrinsic transistor elements. In [2], a seven-element model and exact equations were proposed. However, for the extended model given in Figure 1, the differential resistances R_{fs} and R_{fd} are extracted neglecting the frequency effect on Y-parameters, requiring measurements at very low frequencies [3]. On another work [8], a long procedure based on approximations and an iterative method was proposed.

In this work an alternative method is proposed based on a new set of simple and exact analytical equations. Our method includes the frequency effect in such way that measurements at very low frequency are not necessary, neither long iterative methods nor approximations on frequency.

2. PROPOSED METHODOLOGY

2.1. Extrinsic Elements

Extrinsic inductances (L_s, L_g, and L_d) and resistances (R_s, R_g, and R_d) can be determined using cold bias measurements and Eqs. (1)–(3). These equations represents a simplified transistor model when the gate is forward biased ($V_{gs} > V_{bi}$) and $V_{ds} = 0$ [1]. Extrinsic inductances are obtained from the imaginary part of Eqs. (1)–(3). Additionally, assuming that channel resistance can be neglected [11], extrinsic resistances are calculated from the real part of Eqs. (1)–(3).

$$Z_{11}^{cb} = R_s + R_g + \frac{R_{ch}}{3} + \frac{nkT}{qI_g} + j\omega(L_s + L_g) \quad (1)$$

$$Z_{12}^{cb} = Z_{21}^{cb} = R_s + \frac{R_{ch}}{2} + j\omega L_s \tag{2}$$

$$Z_{22}^{cb} = R_s + R_d + R_{ch} + j\omega(L_s + L_d) \tag{3}$$

where Z_{lm}^{cb}, $l,m = [1,2]$ are impedance parameters obtained from cold-bias measurements, R_{ch} is the channel resistance under the gate, R_s, R_g, and R_d are the extrinsic resistances, $\frac{nkT}{qI_g}$ is the differential resistance of the Schottky diode.

Different methods to determine the parasitic capacitances are presented in [1, 7, 12-15]. In this work, C_{pg} and C_{pd} are determined from Eqs. (4)–(6). These equations are obtained for a simplified transistor model with a reverse biased gate ($V_{gs} < V_p$) and $V_{ds} = 0$, where the intrinsic transistor can be modeled by three identical capacitors, C_b [12].

$$lm\{Y_{11}^{pb}\} = \omega\left(C_{pg} + \frac{2}{3}C_b\right) \tag{4}$$

$$lm\{Y_{12}^{pb}\} = lm\{Y_{21}^{pb}\} = -\omega\frac{C_b}{3} \tag{5}$$

$$lm\{Y_{22}^{pb}\} = \omega\left(C_{pd} + \frac{2}{3}C_b\right) \tag{6}$$

In Eqs. (4)–(6), C_b describe the depletion-layer distribution and Y_{lm}^{pb}, $l,m = \{1,2\}$ are the admittance parameters obtained from pinch-off bias measurements.

2.2. Extended Intrinsic Transistor Model

Once the extrinsic elements were determined, a suitable deembedding process is applied to remove the parasitic pad elements [1]. According with Figure 1, the Y-matrix elements of the intrinsic transistor are given as follow:

$$Y_{11}^{int} = Y_a + Y_c \tag{7}$$

$$Y_{12}^{int} = -Y_a \tag{8}$$

$$Y_{21}^{int} = -Y_a + G_{mo}e^{-j\omega\tau}\left(\frac{1}{1 + j\omega R_i C_{gs}}\right) \tag{9}$$

$$Y_{22}^{int} = Y_a + Y_b \tag{10}$$

where Y_a is the parallel circuit of R_{fd} with the series R_j and C_{gd}:

$$Y_a = \frac{R_j}{R_j^2 + \left(\frac{1}{\omega C_{gd}}\right)^2} + \frac{1}{R_{fd}} + \frac{j\left(\frac{1}{\omega C_{gd}}\right)}{R_j^2 + \left(\frac{1}{\omega C_{gd}}\right)^2} \tag{11}$$

Y_b is the parallel circuit of R_{ds} with C_{ds},

$$Y_b = \frac{1}{R_{ds}} + j\omega C_{ds} \tag{12}$$

and Y_c the parallel circuit of R_{fs} with the series of C_{gs} and R_i,

$$Y_c = \frac{R_i}{R_i^2 + \left(\frac{1}{\omega_{gs}}\right)^2} + \frac{1}{R_{fs}} + \frac{j\left(\frac{1}{\omega C_{gs}}\right)}{R_i^2 + \left(\frac{1}{\omega C_{gs}}\right)^2} \tag{13}$$

We have analyzed Eqs. (7)–(13) and have obtained a new set of exact and simply equations presented in Eqs. (14)–(23), which can be used to determine each one of the equivalent circuit elements. This set of equations requires the Y-parameters of the measured transistor with the extrinsic elements removed. The differential resistances R_{fs} and R_{fd} are determined considering the frequency effect from Eqs. (14) and (15).

$$\mathrm{Re}\{-Y_{12}^{int}\} = R_j C_{gd}[\omega \mathrm{lm}\{-Y_{12}^{int}\}] + \frac{1}{R_{fd}} \tag{14}$$

$$\mathrm{Re}\{Y_{11}^{int} + Y_{12}^{int}\} = R_i R_{gs}[\omega \mathrm{lm}\{Y_{11}^{int} + Y_{12}^{int}\}] + \frac{1}{R_{fs}} \tag{15}$$

The remaining elements of the intrinsic transistor can be determined with the following equations:

$$R_j = \frac{\mathrm{Re}\left\{-Y_{12}^{int} - \frac{1}{R_{fd}}\right\}}{\mathrm{Re}^2\left\{-Y_{12}^{int} - \frac{1}{R_{fd}}\right\} + \mathrm{lm}^2\{-Y_{12}^{int}\}} \tag{16}$$

$$C_{gd} = \frac{\mathrm{Re}^2\left\{-Y_{12}^{int} - \frac{1}{R_{fd}}\right\} + \mathrm{lm}^2\{-Y_{12}^{int}\}}{\omega \mathrm{lm}\{-Y_{12}^{int}\}} \tag{17}$$

$$R_i = \frac{\mathrm{Re}\left\{Y_{11}^{int} + Y_{12}^{int} - \frac{1}{R_{fs}}\right\}}{\mathrm{Re}^2\left\{Y_{11}^{int} + Y_{12}^{int} - \frac{1}{R_{fs}}\right\} + \mathrm{lm}^2\{Y_{11}^{int} + Y_{12}^{int}\}} \tag{18}$$

$$C_{gs} = \frac{\mathrm{Re}^2\left\{Y_{11}^{int} + Y_{12}^{int} - \frac{1}{R_{fs}}\right\} + \mathrm{Im}^2\{Y_{11}^{int} + Y_{12}^{int}\}}{\omega \mathrm{Im}\{Y_{11}^{int} + Y_{12}^{int}\}} \tag{19}$$

$$g_{ds} = \mathrm{Re}\{Y_{22}^{int} + Y_{12}^{int}\} \tag{20}$$

$$C_{ds} = \mathrm{Im}\{Y_{22}^{int} + Y_{12}^{int}\}/\omega \tag{21}$$

$$G_{mo} = \frac{|Y_{21}^{int} - Y_{12}^{int}|}{\mathrm{Im}\{Y_{11}^{int} + Y_{12}^{int}\}}\left(\mathrm{Im}^2\{Y_{11}^{int} + Y_{12}^{int}\} + \mathrm{Re}^2\left\{Y_{11}^{int} + Y_{12}^{int} - \frac{1}{R_{fs}}\right\}\right)^{1/2} \tag{22}$$

$$\tau = \frac{1}{\omega} Tan^{-1}\left(\frac{\begin{array}{c}\mathrm{Im}\{Y_{21}^{int} - Y_{12}^{int}\}\mathrm{Im}\{Y_{11}^{int} + Y_{12}^{int}\} \\ + \mathrm{Re}\left\{Y_{11}^{int} + Y_{12}^{int} - \frac{1}{R_{fs}}\right\}\mathrm{Re}\{Y_{21}^{int} - Y_{12}^{int}\}\end{array}}{\begin{array}{c}\mathrm{Re}\left\{Y_{11}^{int} + Y_{12}^{int} - \frac{1}{R_{fs}}\right\}\mathrm{Im}\{Y_{21}^{int} - Y_{12}^{int}\} \\ - \mathrm{Re}\{Y_{21}^{int} - Y_{12}^{int}\}\mathrm{Im}\{Y_{11}^{int} + Y_{12}^{int}\}\end{array}}\right) \tag{23}$$

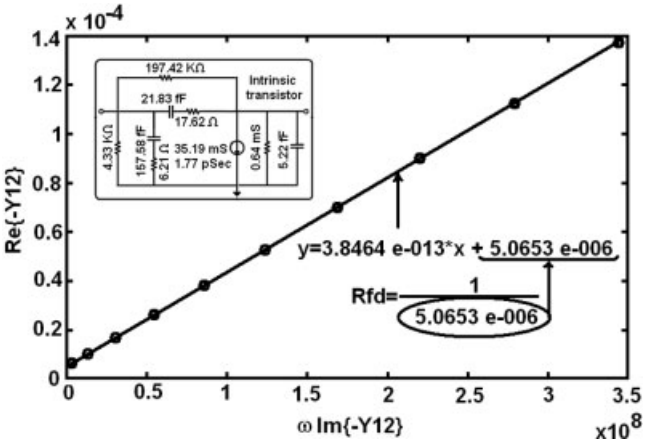

Figure 2 Intrinsic transistor circuit considered in the analysis, including procedure to compute R_{fd}

It is worthy to mention that the difference of the Eqs. (14)–(23) proposed in this work, depends only of the Y-parameters of the intrinsic circuit, whereas the Eqs. (17)–(24) given in [3] depends on element values obtained previously, i.e., R_{gd} (C_{gd}), R_i (C_{gs}), gm (C_{gs} and R_i), and τ (C_{gs}, R_i, and gm).

3. SIMULATION AND EXPERIMENTAL RESULTS

The new proposed methodology to extract the intrinsic elements can be verified first performing an analysis-synthesis process using simulated Y-parameters, starting with a known intrinsic transistor element. Furthermore, to validate the proposed global extraction technique, we have applied it to two microwave FET transistors, where the extracted models are compared with measured data from 1 to 45 GHz.

3.1. Simulation Results

Taken known intrinsic transistor element values from Figure 3 given in Ref. 3, an analysis process to get the intrinsic Y-matrix is performed from 2 to 20 GHz (avoiding measurements at very low frequencies). After that, a synthesis process based on the proposed Eqs. (14)–(23) is carried out as follows: R_{fd} and R_{fs} are obtained from Figures 2 and 3 considering the ordinate at the origin of the straight-line in the graph $\mathrm{Re}\{-Y_{12}^{int}\}$ vs. $\omega\mathrm{Im}\{-Y_{12}^{int}\}$ and $\mathrm{Re}\{Y_{11}^{int}+Y_{12}^{int}\}$ vs. $\omega\mathrm{Im}\{Y_{11}^{int}+Y_{12}^{int}\}$, respectively. As can be seen from Figures 2 and 3, the R_{fd} and R_{fs} values agree with that of Ref. 3, without using measurements at very low frequencies. Besides, extracted elements agree with the known elements given in [3], showing that proposed Eqs. (14)–(23) are exact and consistent with the model. The remaining elements of the model are computed in a straightforward manner using Eqs. (16)–(23).

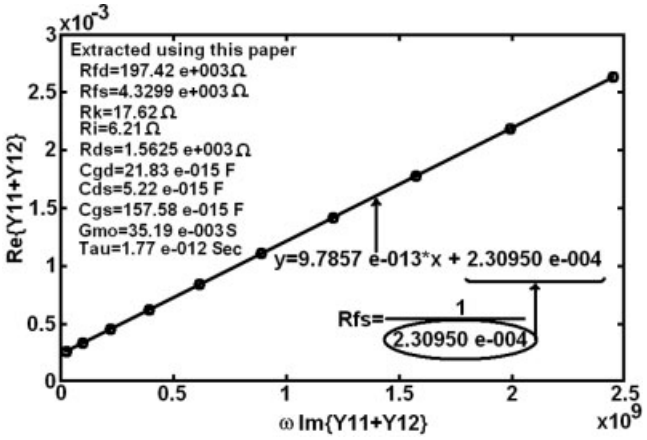

Figure 3 Synthesis results of the analyzed transistor including procedure to determine R_{fs}

3.2. Experimental Results

We verify our method applying it to two different microwave FET transistors. First, a transistor HJFET called FET 1, with a gate length $L_g = 0.2$ μm and a gate width $W_g = 200$ μm was measured and the parasitic pad effects were determined. Then we apply a deembedding to remove their effects from measurement data.

According with Eqs. (14) and (15), in Figures 4 and 5 the measurements follows the predicted linear behavior. R_{fd} and R_{fs} are calculated from Figures 4 and 5 considering the ordinate to the origin of the calculated straight lines, respectively, as the example already shown in Section 3.1. As can be clearly observed in Figures 4(a) and 5(a), the bias effect is weakly on the R_{fd} value, however, it is strongly reflected on R_{fs}.

In Table 1, the extracted elements are listed for two representative bias points: (1) $V_{ds} = 2$ V, $I_{ds} = 5$ mA; and (2) $V_{ds} = 2$ V, $I_{ds} = 10$ mA. Additionally, results for another measured transistor type P-HEMT called FET 2, with $L_g = 0.15$ μm and $W_g = 120$ μm are also included in Table 1. We can note that R_{fd} is always higher than R_{fs}, and that both resistances increase also with bias current. Generally, both resistances have high values, which are consistent with the transistor circuit. When R_{fs} and R_{fd} take very high values,

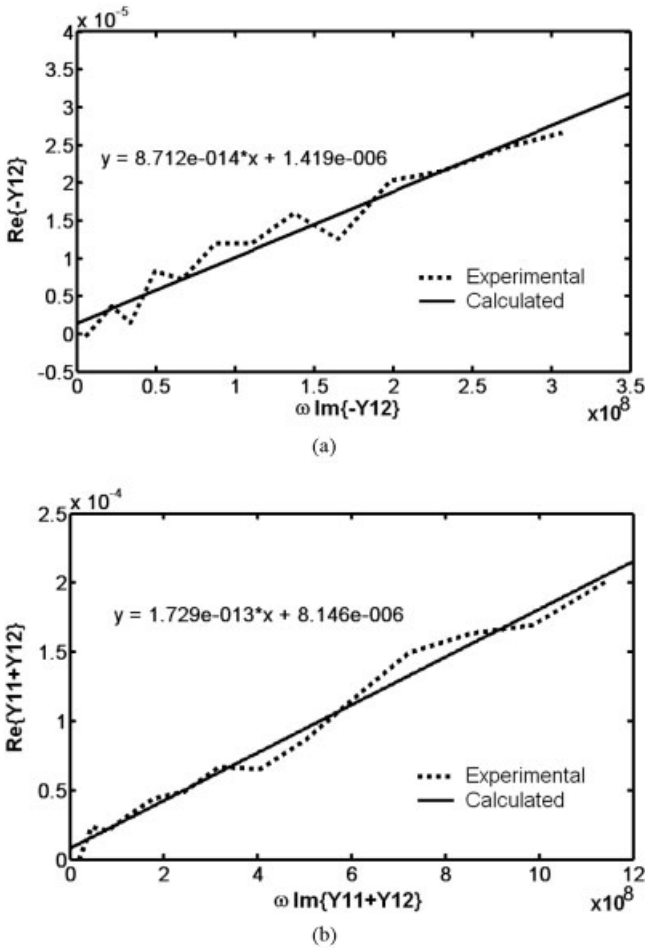

Figure 4 Experimental data and calculated straight line for determining (a) R_{fd} and (b) R_{fs} for FET 1 at 2 V and 5 mA

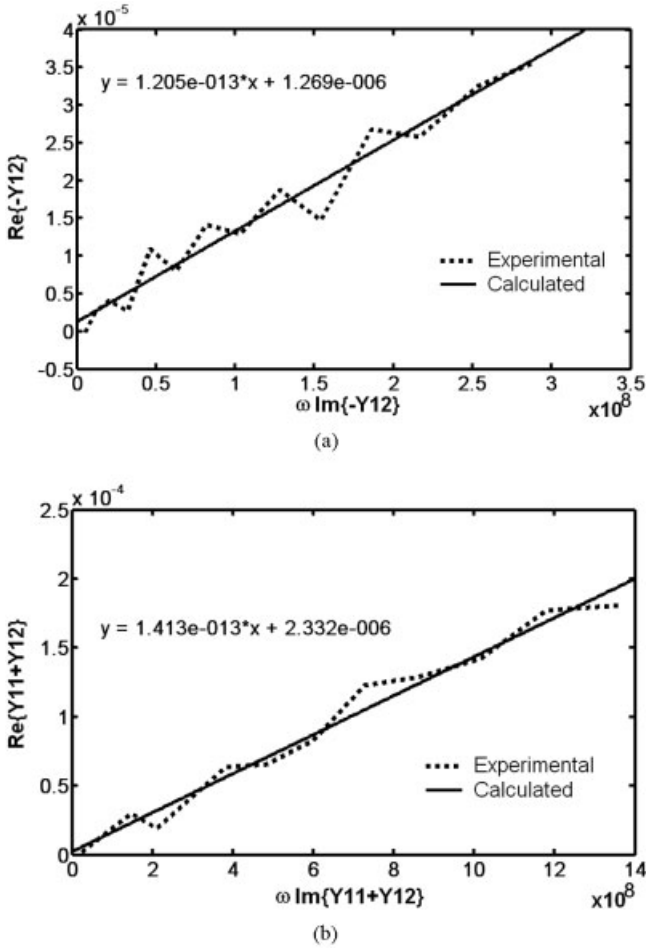

Figure 5 Experimental data and calculated straight line for determining (a) R_{fd} and (b) R_{fs} for FET 1 at 2 V and 10 mA

the conductance gfd ($= 1/R_{fd}$) and gfs ($= 1/R_{fs}$) [ordinate to origin in Eqs. (14) and (15)] are extremely low tending to zero or less than zero (negative).

Figures 6 and 7 depict a comparison of measured versus modeled S-parameters from 1 to 45 GHz for the FET1 and for FET 2, respectively, at the same bias point $V_{ds} = 2$ volts and $I_{ds} = 5$ mA. Excellent agreement between measurement and modeled data is obtained. In Figure 6, the worst-case magnitude relative error is 4% for S_{22} at frequencies lower than 4 GHz. The worst case for the phase difference is 3° in the S_{22} at frequencies higher than 40 GHz, however, at frequencies below 40 GHz the maximum phase difference is 1.5°. Similar errors were obtained for the S parameters of the transistor shown in Figure 7.

TABLE 1 Extracted Small-Signal Model Parameters

	FET 1		FET 2	
Element	2 V, 5 mA	2 V, 10 mA	2 V, 5 mA	2 V, 10 mA
R_{fd} (kΩ)	704.8087	788.1124	347.7425	498.1827
R_j (Ω)	5.7084	7.7436	0.6540	1.5681
C_{gd} (fF)	34.9878	32.8565	32.0610	30.6844
R_{ds} (Ω)	273.3547	186.6378	234.8803	164.1503
C_{ds} (fF)	47.9183	51.2623	42.7789	45.7435
R_i (Ω)	1.6417	1.2980	0.1069	0.2907
R_{fs} (kΩ)	122.7611	428.8732	98.1471	100.5423
C_{gs} (fF)	130.2206	156.5634	75.6474	86.9177
G_{mo} (ms)	49.0776	76.4761	47.2922	71.5280
T (ps)	0.6573	0.5294	0.2626	0.1866
R_g (Ω)	1.2119		1.2555	
R_d (Ω)	3.7861		4.9433	
R_s (Ω)	2.3534		3.8366	
C_{pg} (fF)	6.2415		15.3643	
C_{pd} (fF)	11.0866		12.2705	
L_g (pH)	22.5237		22.7108	
L_d (pH)	34.5886		29.9768	
L_s (pH)	3.5248		8.8847	

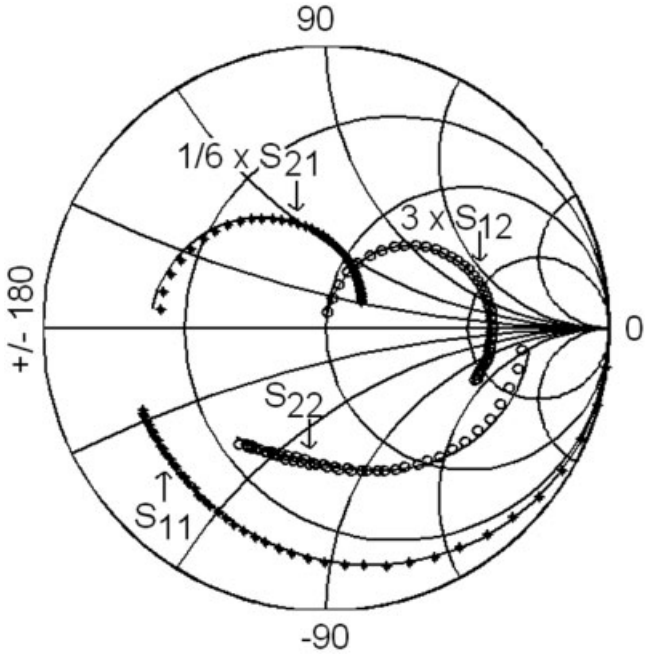

Figure 6 Measured (o,*) vs. modeled (−) S-parameters up to 45 GHz for FET 1 at $V_{ds} = 2$ V and $I_{ds} = 5$ mA

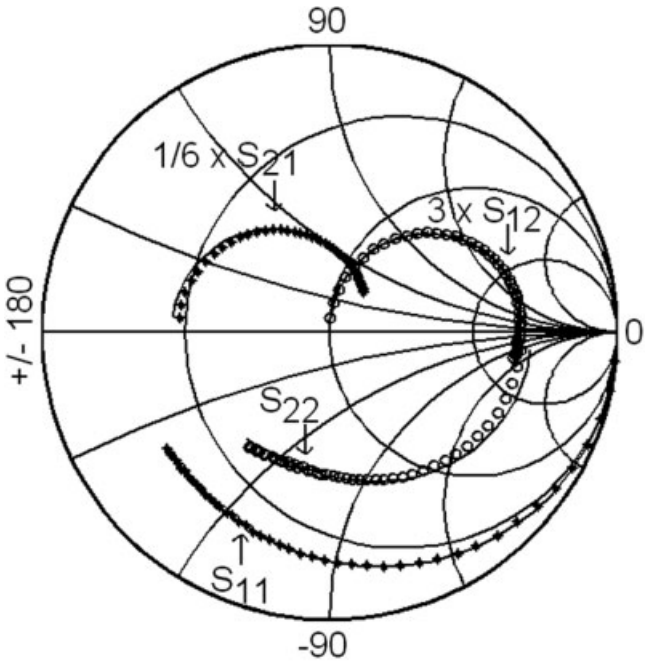

Figure 7 Measured (o,*) vs. modeled (−) S-parameters up to 45 GHz for FET 2 at $V_{ds} = 2$ V and $I_{ds} = 5$ mA

Although resulting errors are very small, we have noted that accuracy depends strongly on the extrinsic parasitic extraction method used to obtain the extrinsic capacitances (C_{pg} and C_{pd}) and resistances (R_g, R_s, and R_d).

4. CONCLUSION

We have presented a new methodology to determine the small signal equivalent circuit for microwave FET transistors. We have proposed a new set of simple equations to obtain the intrinsic transistor elements of the extended transistor model. These equations are based only on Y-parameters and on differential resistances R_{fs} and R_{fd}. The proposed methodology to determine R_{fs} and R_{fd} includes the frequency effect in such way that measurements at very low frequencies are not required. Our method was implemented and the equivalent circuit elements for different microwave transistors have been presented. The validity of our method is certified by a direct comparison of measured S-parameters vs. model results, showing a very good agreement of a few percent up to 45 GHz.

ACKNOWLEDGMENT

This work was partially supported by CONACYT under grant 35225A and a PhD scholarship.

REFERENCES

1. G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, A new method for determining the FET small-signal equivalent circuit, IEEE Trans Microwave Theory Tech MTT-36 (1988), 1151-1159.
2. M. Berroth and R. Bosch, Broad-band determination of the FET small-signal equivalent circuit, IEEE Trans Microwave Theory Tech MTT-38 (1990), 891-895.
3. M. Berroth and R. Bosch, High-frequency equivalent circuit of GaAs FET's for large-signal applications, IEEE Trans Microwave Theory Tech MTT-39 (1991), 224-229.
4. B.L. Ooi, J.Y. Ma, An improved but reliable model for MESFET parasitic capacitance extraction, IEEE Radio Frequency Integrated Circuit Symposium, Philadelphia, PA 2003, pp. 567-570.
5. C.F. Campbell and S.A. Brown, An analytic method to determine GaAs FET parasitic inductances and drain resistance under active bias conditions, IEEE Trans Microwave Theory Tech MTT-49 (2001), 1241-1247.
6. D. Costa, W.U. Liu, and J.S. Harris, Direct extraction of the AlGaAs heterojunction bipolar transistor small-signal equivalent circuit, IEEE Trans Electron Devices (1991), 2018-2024.
7. Y. Gobert, P.J. Tasker, and K.H, Bachem, A physical, yet simple, small-signal equivalent circuit for the Heterojunction bipolar transistor, IEEE Trans Microwave Theory Tech MTT-45 (1997), 149-153.
8. A. Miras and E. Legros, Very high-frequency small-signal equivalent circuit for short gate-length InP HEMT, IEEE Trans Microwave Theory Tech MTT-45 (1997), 1018-1026.
9. R. Tayrani, J.E. Gerber, T. Daniel, R.S. Pengelly, and U.L. Rohde, A new and reliable direct parasitic extraction method for MESFETs and HEMTs, Proceedings of the 23rd European Microwave Conference, 1993, pp. 451-453.
10. M.C.A.M. Koolen, J.A.M. Geelen, and M.P.J.G. Versleijen, An improved de-embedding technique for on-wafer high-frequency characterization, Proceedings of the IEEE Bipolar Circuits and Technology Meeting, 1991, pp. 188-191.
11. J.A. Reynoso-Hernández, F.E. Rangel-Patiño, and J. Perdomo, Full RF characterization for extraction the small-signal equivalent circuit in microwave FET's, IEEE Trans Microwave Theory Tech MTT-40 (1996), 2625-2633.
12. P.M. White and R.M. Healy, Improved equivalent circuits for determination of MESFET and HEMT parasitic capacitances from 'cold-fet' measurements, IEEE Microwave Guided Wave Lett 12 (1993), 453-454.
13. Y. Lai and K. Hsu, A new pinched-off cold-FET method to determine parasitic capacitances of FET equivalent circuits, IEEE Trans Microwave Theory Tech MTT-49 (2001), 1410-1418.
14. W.R. Curtice and R.L. Camisa, Self-consistent GaAs FET models for amplifier design and device diagnostics, IEEE Trans Microwave Theory Tech MTT-32 (1984), 1573-1578.
15. K. Shirakawua, H. Oikawua, T. Shimura, Y. Kawasaki, Y. Ohashi, T. Saito, Y. Daido, An approach to determining an equivalent circuit for HEMT's, IEEE Trans Microwave Theory Tech MTT-43 (1995), 499-503.

DESIGN OF A 3–10 GHZ UWB CMOS T/R SWITCH

K.-H Pao,[1] C.-Y. Hsu,[1] H.-R. Chuang,[1] and C.-Y Chen[2]

[1] Department of Electrical Engineering, Institute of Computer and Communication Engineering, National Cheng Kung University, Tainan, Taiwan, Republic of China; Corresponding author: k1006849@ms18.hinet.net

[2] Department of Electronic Engineering, National University of Tainan, Tainan, Taiwan, Republic of China

Received 14 July 2007

ABSTRACT: *A 3–10 GHz broadband CMOS T/R Switch for ultra-wideband (UWB) transceiver is proposed. This broadband CMOS transmit/receive (T/R) Switch is fabricated based on the 0.18 μm 1P6M standard CMOS process. On-chip measurement of the CMOS T/R Switch is performed. The insertion loss of the proposed CMOS T/R Switch is about 3.1 ± 1.3 dB. The return losses at both input and output terminals are higher than 14 dB. It is also characterized with 25–34 dB isolation and 18–20 dBm input P_{1dB}. The broadband CMOS T/R Switch shows highly linear phase and group delay of 20 ± 10 ps from 10 MHz to 15 GHz. It can be easily integrated with other CMOS RFICs to form on-chip transceivers for various UWB applications.* © 2007 Wiley Periodicals, Inc. Microwave Opt Technol Lett 50: 457–460, 2008; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.23129

Key words: *CMOS; transmit/receive (T/R) switch; ultra-wideband (UWB); lowpass filter*

1. INTRODUCTION

Recently, GaAs technology has been extensively implemented in many RF/microwave switch modules. To consider the cost down and system integration, it is desirable to use standard CMOS process for implementation of high-performance wide band T/R switch. Several T/R switches using CMOS technology have been developed [1–7]. But they are all operated in narrow band. In general, CMOS RF switches are usually operated less than 3 GHz. For UWB radio frequency or higher frequency applications, most switches made by Pin Diode and GaAs are demonstrated.

An UWB 3–10 GHz CMOS RF SDPT Switch based on CMOS 0.18 μm process is proposed in this letter. The concepts of distributed circuit and ladder type low-pass filter are adopted to design the CMOS T/R switch. The proposed CMOS T/R switch has about 3 dB insertion loss and 28 dB isolation from 3 to10 GHz. The input and output return losses are better than 14 dB. It also has highly linear phase and group delay. Compared with the GaAs switches, the CMOS switches not only